

FIG. 1

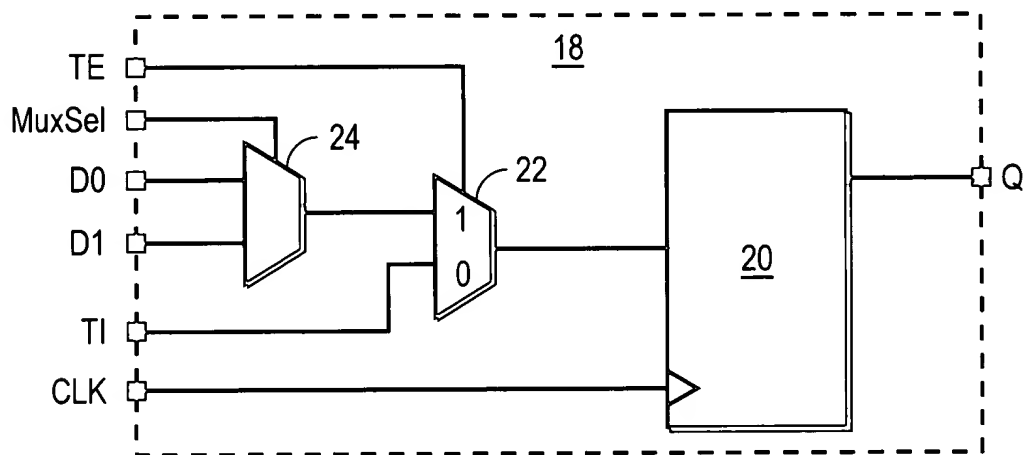


FIG. 2

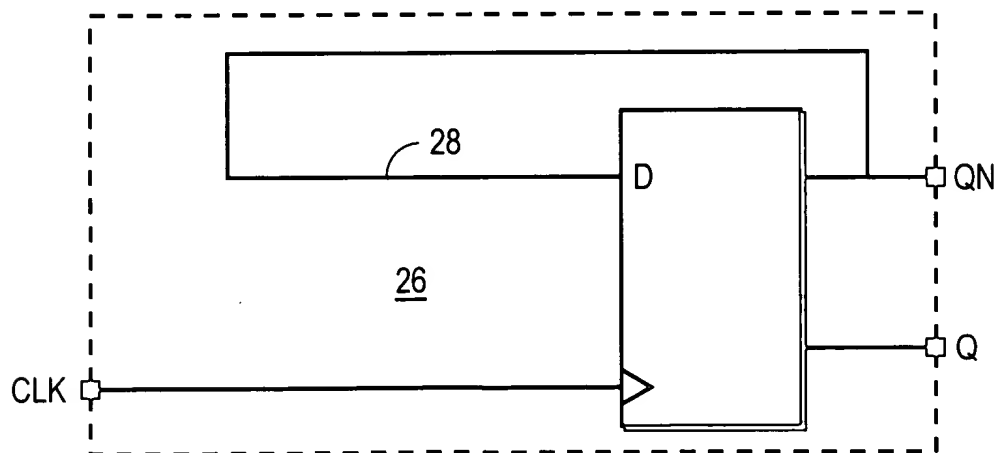


FIG. 3

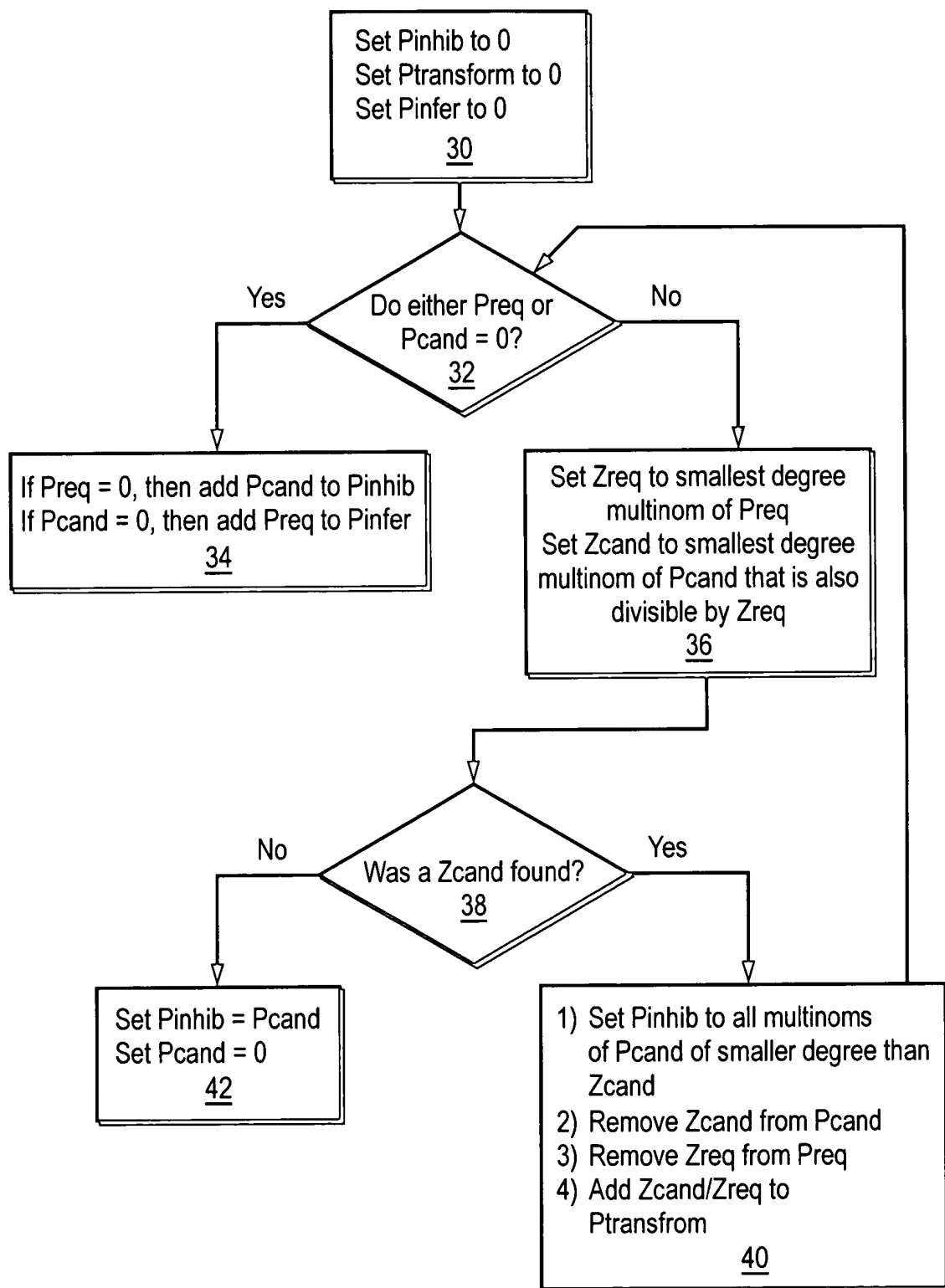


FIG. 4

Inhibition	
<b>Rst</b>	inhib a Reset active high
<b>RstLr</b>	inhib a Reset active low
<b>St</b>	inhib a Set active high
<b>StLs</b>	inhib a Set active low
<b>ScStRst</b>	inhib a Scan active high
<b>ScStLsRstLc</b>	inhib a Scan active low
<b>MuScStRst</b>	inhib a Mux
<b>Re</b>	inhib a Recirculating active high
<b>ReLre</b>	inhib a Recirculating active low
<b>T</b>	stop proces, impossible to inhib a Toggle element

FIG. 5

Transformation	
rule 1	<b>1</b> : Do nothing
rule 2	<b>Ls or Ls<sup>-1</sup></b> : Add an inverter on the Reset terminal
rule 3	<b>Lr or Lr<sup>-1</sup></b> : Add an inverter on the Set terminal
rule 4	<b>Lre or Lre<sup>-1</sup></b> : Add an inverter on the Recirculating enable
rule 5	<b>LrLs or (LrLs)<sup>-1</sup></b> : Add an inverter on the Scan enable
rule 6	<b>ScSt</b> : set TI to Vss and connect TE to Reset terminal
rule 7	<b>ScRst</b> : set TI to Vss and connect TE to Set terminal
rule 8	<b>ScRst(Ls<sup>-1</sup>)</b> : set TI to Vdd and connect TE to set terminal with an inverter
rule 9	<b>ScSt(Lr<sup>-1</sup>)</b> : set TI to Vss and connect TE to reset terminal with an inverter
rule 10	<b>ScStLrLs</b> : set TI to Vss and connect TE to reset terminal with an inverter
rule 11	<b>ScRstLrLs</b> : set TI to Vdd and connect TE to set terminal with an inverter
rule 12	<b>ScRstLr</b> : set TI to Vdd and connect TE to set terminal
rule 13	<b>ScStLs</b> : set TI to Vss and connect TE to reset terminal
rule 14	<b>Mu</b> : connect D1 to TI and connect SEL to TE terminal
rule 15	<b>Mu(LrLs)<sup>-01</sup></b> : connect D0 to TI and connect SEL to TE terminal
rule 16	<b>MuScSt</b> : set D1 to Vss and connect SEL to Reset terminal
rule 17	<b>MuScRst</b> : set D1 to Vdd and connect SEL to set terminal
rule 18	<b>MuScRst(Ls<sup>-1</sup>)</b> : set D0 to Vdd and connect SEL to set terminal
rule 19	<b>MuScSt(Lr<sup>-1</sup>)</b> : set D0 to Vss and connect SEL to set terminal
rule 20	<b>Mu<sup>-1</sup></b> : connect D1 to TI, SEL to TE
rule 21	<b>(Mu<sup>-1</sup>)LsLr</b> : connect D0 to TI, SEL to TE

FIG. 6

Inference	
<b>Rst</b>	infer a Reset active high
<b>RstLr</b>	infer a Reset active low
<b>St</b>	infer a Set active high
<b>StLs</b>	infer a Set active low
<b>ScStRst</b>	infer a Scan active high
<b>ScStLsRstLr</b>	infer a Scan active low
<b>MuScStRst</b>	infer a Mux
<b>Re</b>	infer a Recirculating active high
<b>ReLre</b>	infer a Recirculating active low
<b>T</b>	infer a Toggle element

FIG. 7

row/column	Rst	RstLR	St	StLs	ScStRst	ScStLsRstLr	MuScStRst	Re	ReLre	T
Rst	T1	T2	----	----	----	----	----	----	----	----
RstLr	T2	T1	----	----	----	----	----	----	----	----
St	----	----	T1	T3	----	----	----	----	----	----
StLs	----	----	T3	T1	----	----	----	----	----	----
ScStRst	T6	T9	T7	T8	T1	T5	T20	----	----	----
ScStLsRstLr	T10	T13	T11	T12	T5	T1	T21	----	----	----
MuScStRst	T16	T19	T17	T18	T14	T15	T1	----	----	----
Re	----	----	----	----	----	----	----	T1	T4	----
ReLre	----	----	----	----	----	----	----	T4	T1	----
T	----	----	----	----	----	----	----	----	----	T1

FIG. 8

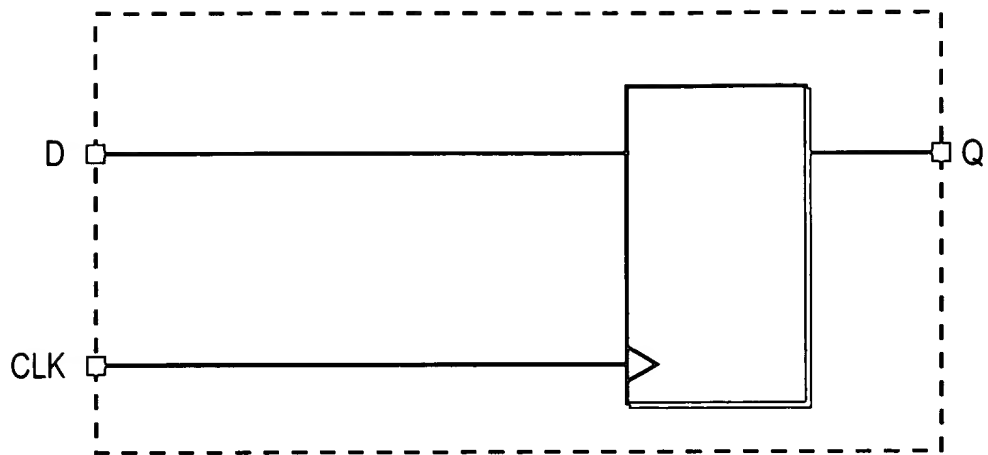


FIG. 9

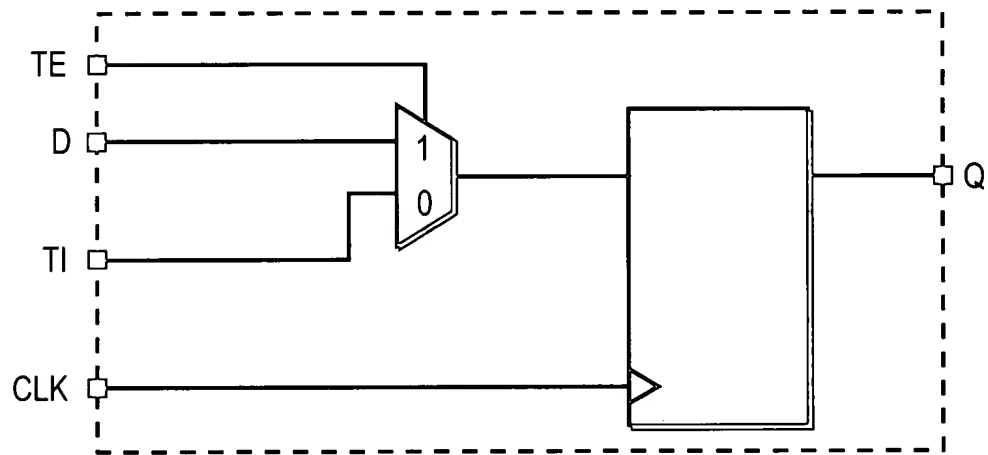


FIG. 10

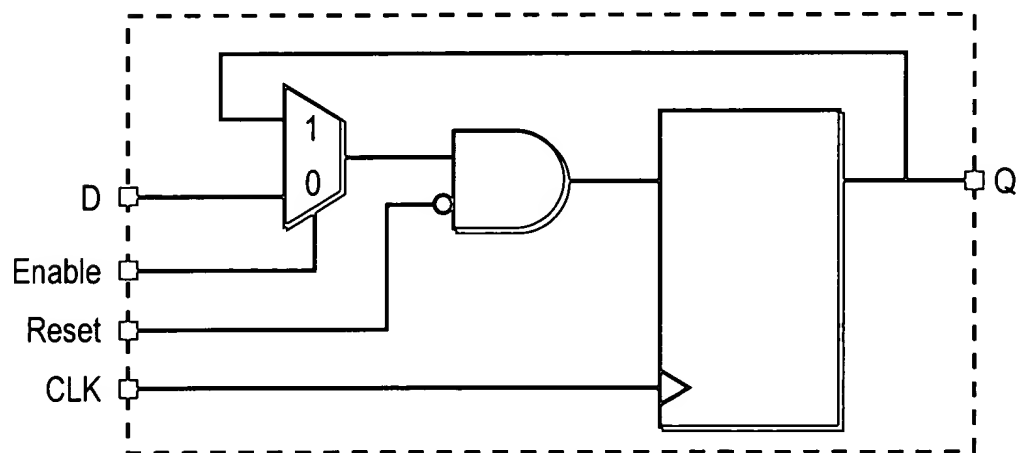


FIG. 11